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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/436,062	11/08/1999	CRAIG W. WARNER	10991087-1	6095

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EXAMINER	
FERRIS, DERRICK W	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 12/17/2003

11

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/436,062	WARNER, CRAIG W.	
	Examiner	Art Unit	
	Derrick W. Ferris	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/15/03 has been entered.

Response to Amendment

2. **Claims 1-17,19-22, and 24-25** as amended are still in consideration for this application. Applicant has amended claims 1, 2, 5-7, 10-12, 14-16, 19, 20, and 25. Applicant has canceled claims 18 and 23.

3. Examiner **withdraws** the obviousness rejection to *Galles* for Office action filed 05/27/2003. Based on the claims as necessitated by amendment, a new rejection has been made. In addressing applicant's arguments in the response filed 07/15/03, the examiner notes three main items of issue: (1) source logic in the source node to identify a data route from the source node to the destination node, (2) a total number of hops in the data route (i.e., the total number of hops field) and (3) a packet header attached to a packet that specifically contains (a) an egress port of a next subsequent node, (b) current hop count, and (c) total number of hops (i.e., a header that contains elements (a), (b), and (c)).

In reference to (1) source logic in the source node to identify a data route from the source node to the destination node, examiner notes *Galles* teaches routing a packet based on a local routing table such that each router along the path consults a routing table (e.g., see at least

column 1, lines 59-64). In addition, please see at least column 2, lines 29-38 (emphasis added) with respect to pipelining where the header already contains the egress port identifier of the current router. In other words, the route is already predefined by the source node and is updated if necessary by each router via the local routing tables (e.g., see at least column 16, lines 25-35). Thus *Galles* teaches the limitation of source logic in the source node to identify a data route from the source node to the destination node.

The examiner has further strengthened the argument for (2) and (3). In particular, examiner claims that an egress port of (a) a next subsequent node, (b) current hop count, and (c) total number of hops are shown for a vector packet (i.e., (a), (b), and (c) are now anticipated by the reference as opposed to previously where they would have been obvious to one skilled in the art). In assisting with the rejection, the examiner will now draw an analogous relationship between applicant's figure 3 and figures 13 and 17 of *Galles*. In particular, note a second destination port 149b of applicant (see applicant's figure 3) as vector 1312b of *Galles*, a first destination port 149a of applicant as vector port 1312a, a current hop count 146 of applicant as shown as part of the vectors in figure 13 and more in detail in figure 17 and a total hop count 143 of applicant shown in figure 13 and more in detail in figure 17 as part of the vectors. Specifically for the vectors, a current hop count 146 and a total hop count 143 are derived from figure 17 based on the positioning of the vectors (e.g., see the example presented in section 4.5.1 starting at column 18). Examiner notes that not clearly shown in figure 13 of *Galles* is whether the vectors are part of a packet header. Examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to consider the vectors as part of the header. Examiner notes a motivation for considering the vector as part of the header is that the vector

contains "routing information" which is typically placed in the header portion of packet as is known by someone skilled in the art. Specifically, the routing formation (i.e., the port information) is typically contained in the packet header. Furthermore, examiner notes that the information is clearly not placed in the data/payload portion of the packet as shown in figure 13. To further cure the above-cited deficiency, *Stallings* teaches that it is well known in the art to put a total hop count as well as routing information into a packet header such as an IP header (e.g., see figure 16.7 on page 544 where the TTL contains the router hops). Thus *Stallings* provides the support and motivation for why someone skilled in the art would place an egress port, a current hop count and total hop count in a packet header.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1-17 and 19-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No., 5,721,819 to Galles et al. ("*Galles*") in view of "Data and Computer Communications" to *Stallings*.

As to **claims 1, 6, 11 and 16**, *Galles* discloses a programmable distributed routing system and method using routing tables for a network in general, and more specifically towards a multi-processor environment [column 1, lines 16-24]. As applicant's invention is also directed towards routing in a multi-processor environment, examiner notes a strong motivation for using the subject matter as a whole for the reference. Using the

example shown in figures 16 and 17, examiner notes *Galles* discloses a number of nodes such as a source node (e.g., an originating device 1604), an intermediate node (e.g., router 204c), and a destination node (e.g., target device 1608) [column 18, lines 1-60]. Examiner notes that *Galles* discloses in general, using a broad but reasonable interpretation, source logic, routing logic, and destination logic (also referred to as path identification means, routing means and destination means) to identify, transmit, route, and detect respectively. In particular, each of the nodes has an ingress port and an egress port (note that one skilled in the art would recognize that originating device 1604 and target device 1608 have both an ingress and egress port depending on the path of the packet as shown in relation to figures 16 and 18). With respect to source logic also see at least column 16, lines 25-45 of *Galles*. With respect to the elements of a header containing an egress port of a next subsequent node, a current hop count, and a total hop count see at least figures 13 and 17 where an egress port is shown as a vector field, and a current hop count and total hop count are easily derived from the port vectors.

Not clearly taught by *Galles* is the further limitation of a data packet header that contains the elements mentioned previously for a packet header. In particular, it is unclear from figure 13 whether the vector information is located within the header or attached to the packet. Examiner notes that it would have been obvious to someone skilled in the art prior to applicant's invention to use a packet header that contains at least an egress port of a next subsequent node, a current hop count, and a total hop count. One skilled in the art would be motivated to place the vector information in the header portion since the header portion typically contains "routing information" such as address

information and hop count. As further support, *Stallings* cures the above-cited deficiency by teaching that it is well known in the art to put a total hop count as well as routing information into a packet header such as an IP header (e.g., see figure 16.7 on page 544 where the TTL contains the router hops). One motivation for placing this information in a header is so the router can easily locate information within a defined packet structure. Thus *Stallings* provides the support and motivation for why someone skilled in the art would place an egress port, a current hop count and total hop count in a packet header. Furthermore, *Stallings* provides further motivation by disclosing that hop counts are represented as a single field as opposed to being derived from the vector information (e.g., see the TTL field in the IP header in figure 16.7).

As to **claims 2 and 7**, examiner notes this example also shows a return route path [column 18, lines 62-67; column 19, lines 1-25]. Noted specifically is the source port stored in the vector packet configuration. Examiner also notes a total hop count is shown (see reasoning in rejection for claim 1).

As to **claims 3 and 8**, *Galles* discloses a routing table for each router (including a source node).

As to **claims 4 and 9**, examiner notes the reasoning behind the rejection for claim 1 shows that it would have been obvious to a skilled artisan to decrement the hop count (indirectly).

As to **claims 5 and 10**, *Galles* broadly discloses replacing the destination port with the source port of the intermediate node (e.g., see figure 17). In particular, the

threshold is reached when the END value is reached with respect to the port vectors (i.e., examiner notes a reasonable but broad interpretation of port vectors).

As to **claim 12**, again as mentioned in the rejection for claim 12, it would have been obvious to a skilled artisan prior to applicant's invention to include a total hops value (i.e., same motivation applies). *Galles* also broadly discloses recording at least one source port value in the data packet (for the return path).

As to **claim 13**, *Galles* discloses at least one routing path between source and destination node.

As to **claim 14**, examiner notes that it would have been obvious to a skilled artisan prior to applicant's invention to decrement the current hop count (see the reasoning behind the rejection for claim 11 in that the same motivation applies).

As to **claim 15**, see the reasoning behind the rejection for claim 13. Again, *Galles* broadly discloses an act of replacing.

As to **claim 17**, figure 17 clearly shows when a packet has arrived at the destination node (i.e., target device 1608).

As to **claim 19**, examiner notes that a header 1304 can further contain a source port value (i.e., ingress port) for the purpose of re-routing [column 18, lines 34-37].

As to **claims 20-22**, as shown in figure 17, the receipt may be acknowledged using the alterative embodiment by swapping the destination and source port values using a reasonable but broad interpretation of "swapping". Examiner notes that the same reasoning also applies with respect to hop count as mentioned in the rejection for claim 1.

Examiner also notes that the return routing is performed independently of the routing table [column 18, lines 61-67; column 19, lines 1-25].

6. **Claims 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No., 5,721,819 to Galles et al. ("*Galles*") in view of "Data and Computer Communications" to *Stallings*, and in further view of "A Queuing Model for Wormhole Routing with Timeout" to *Hu et al.* ("*Hu*")

As to **claim 24**, *Galles* is silent or deficient to checking for a time-out value in general. Examiner notes that it would have been obvious to a skilled artisan prior to applicant's invention to use a time-out value in general to avoid deadlock problems in a multiprocessor network. As further support, *Hu* discloses using a time-out to avoid deadlock [page 585].

As to **claim 25**, *Hu* is silent or deficient to the type of routing algorithm employed (i.e., the routing strategy is not specified) [page 585] such that it would have been obvious to a skilled artisan to use a routing algorithm to avoid deadlock free routing. *Galles* discloses performing deadlock free routing [column 2, lines 4-5] such that routing tables can be reprogrammed to account for changes in the network configuration such as deadlock.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (703) 305-4225. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

Derrick W. Ferris
Examiner
Art Unit 2663

DWF

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 12/10/03